

# Model Name: GA-VM900M

Revision :1.0

SHEET	TITLE
1	BOM & PCB MODIFY HISTORY
2	COVER SHEET
3	BLOCK DIAGRAM
4,5,6,7	INTEL P4_LGA775 CPU
8,9,10,11	P4M900 (NORTH BRIDGE)
12	CLOCK GENERATOR (ICS953002DF+9P956AF)
13,14,15	VT8237A (SOUTH BRIDGE)
16,17	DDR II SDRAM DIMMS 1,2 DDR TERMINATION
18	PCI Express x16
19	PCI SLOT 1,2,PCI_E x1
20	BIOS , VGA Connect
21	IDE,USB
22	LPC I/O_W83627DHG
23	COM,PRT,FDD,KB/MS
24	VT1708A CODEC
25	AUDIO JACK
26	PANEL,FANS
27	LAN RTL8201CL & USB CONNECTOR
28	DDR POWER
29	ATX CONN,3VDUAL,VDDQ DC POWER
30	VCORE PWM ISL6312CRZ

GIGABYTE		
Title		
COVER SHEET		
Size	Document Number	Rev
Custom	GA-VM900M	1.0
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**Model Name: GA-VM900M**

**Version:1.0**

### Component value change history

**P-code:A95120-0      2006.06.30**

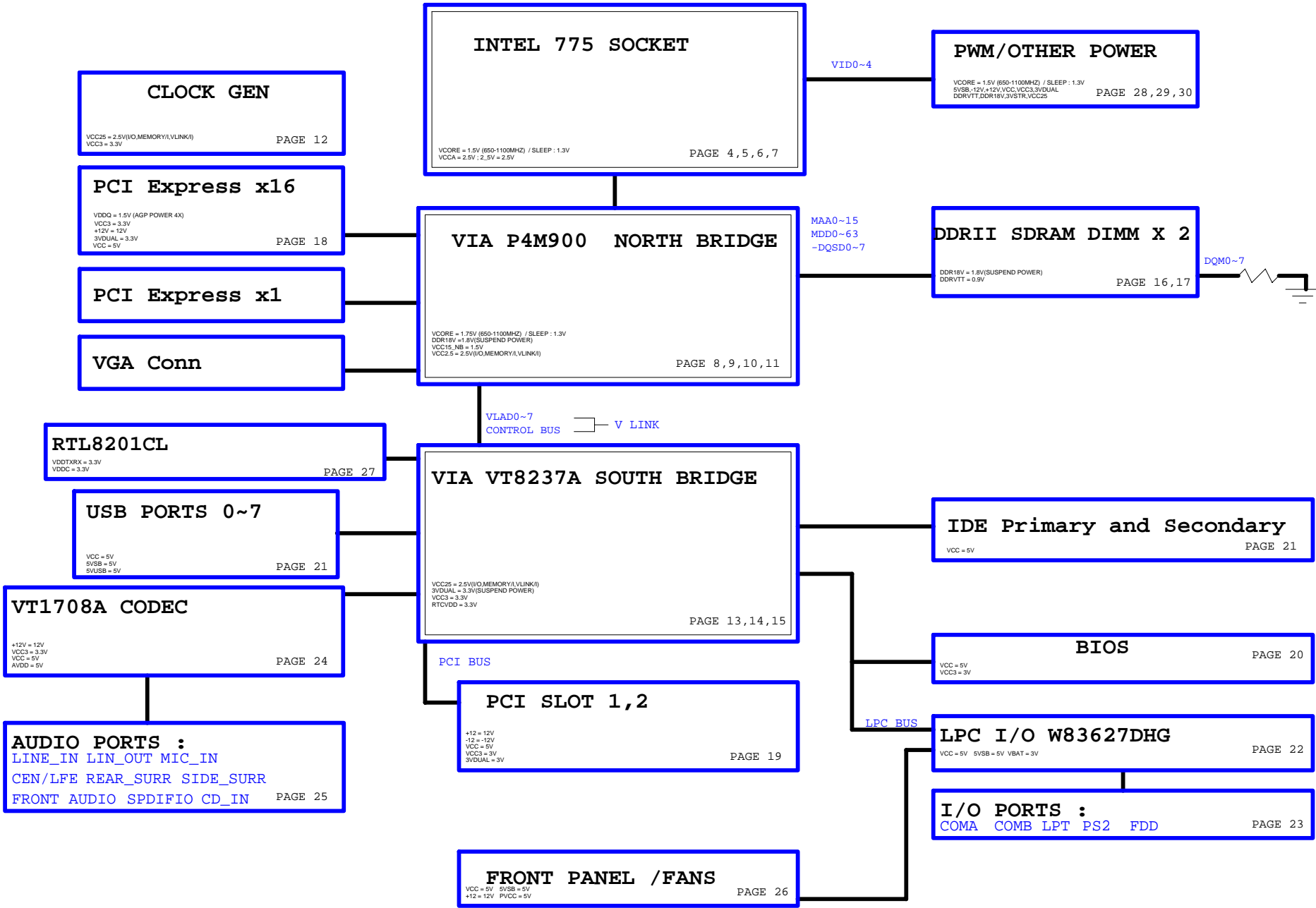
[illegible]

### Circuit or PCB layout change for next version

[illegible]

<b>GIGABYTE</b>			
<b>BOM &amp; PCB MODIFY HISTORY</b>			
Title			
Size Custom	Document Number  <b>GA-VM900M</b>	Rev  <b>1.0</b>	
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# BLOCK DIAGRAM



GIGABYTE		
Title	BLOCK DIAGRAM	
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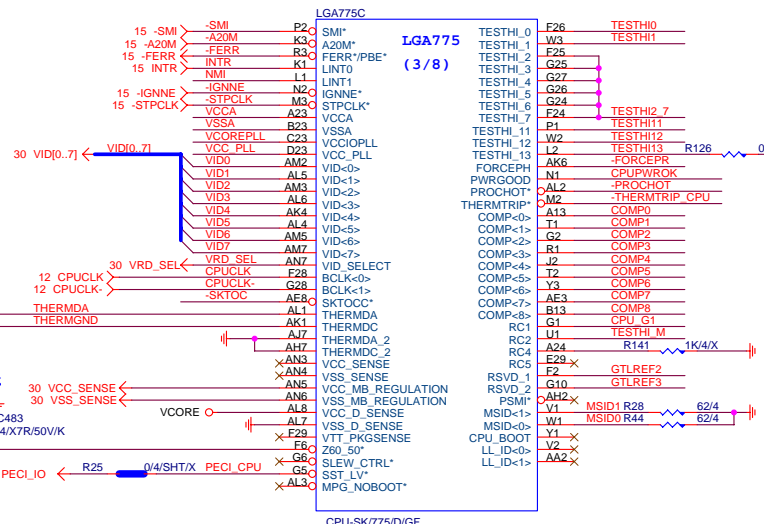
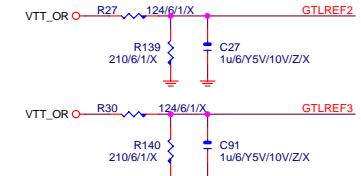
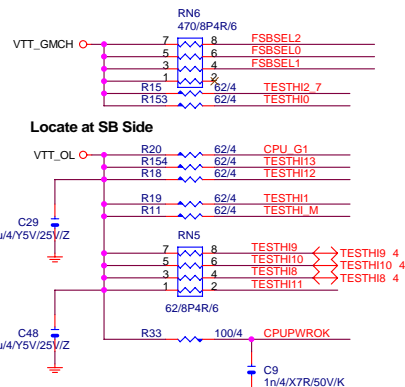
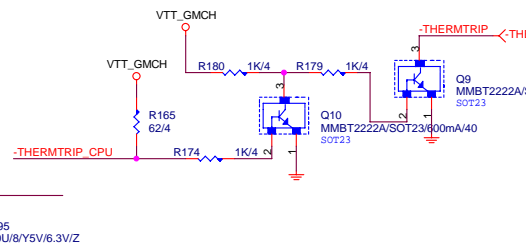


<b>GIGABYTE</b>				
Title				
P4_LGA775-C				
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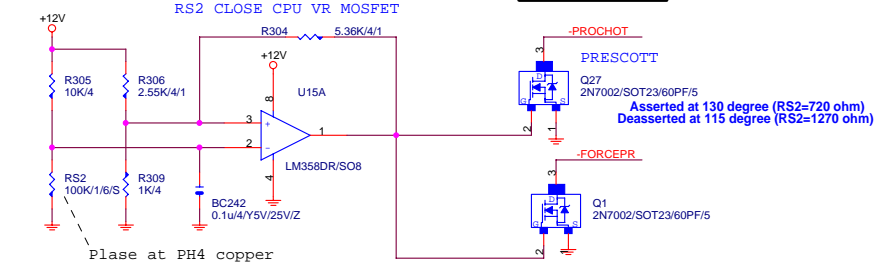
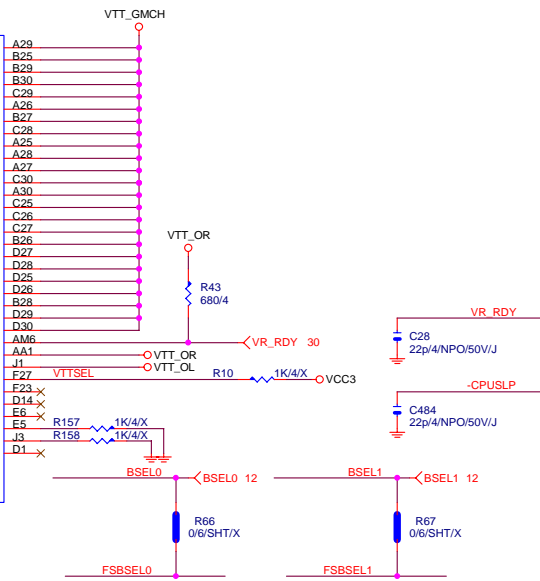
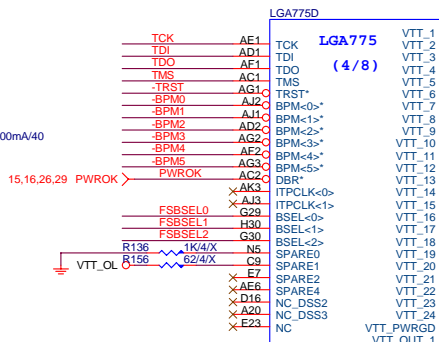
**Note:** VCCA & VCOREPLL define doesn't same as old P4 design kit

As close as possible to CPU socket

As close as possible to  
CPU socket



**X**

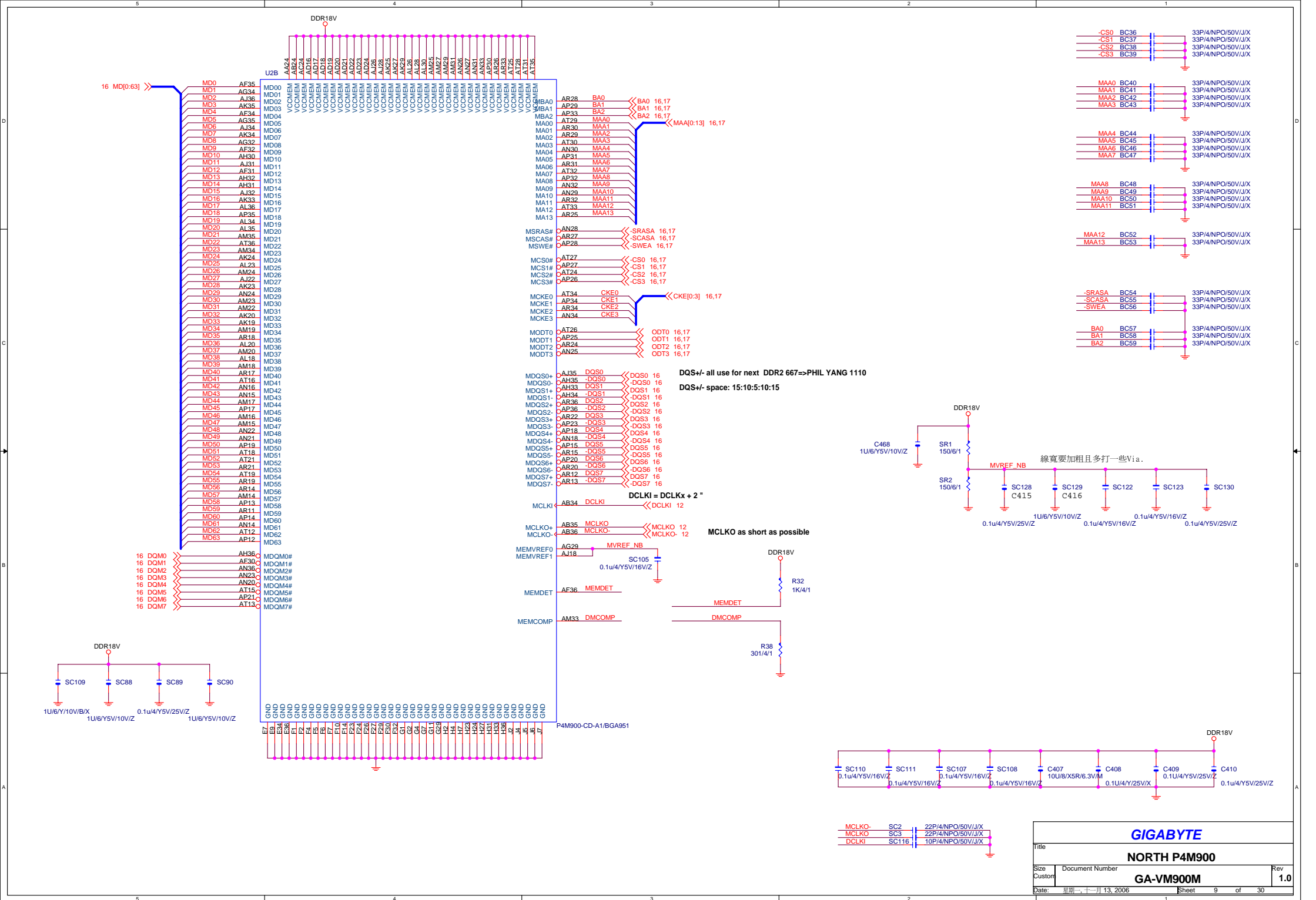


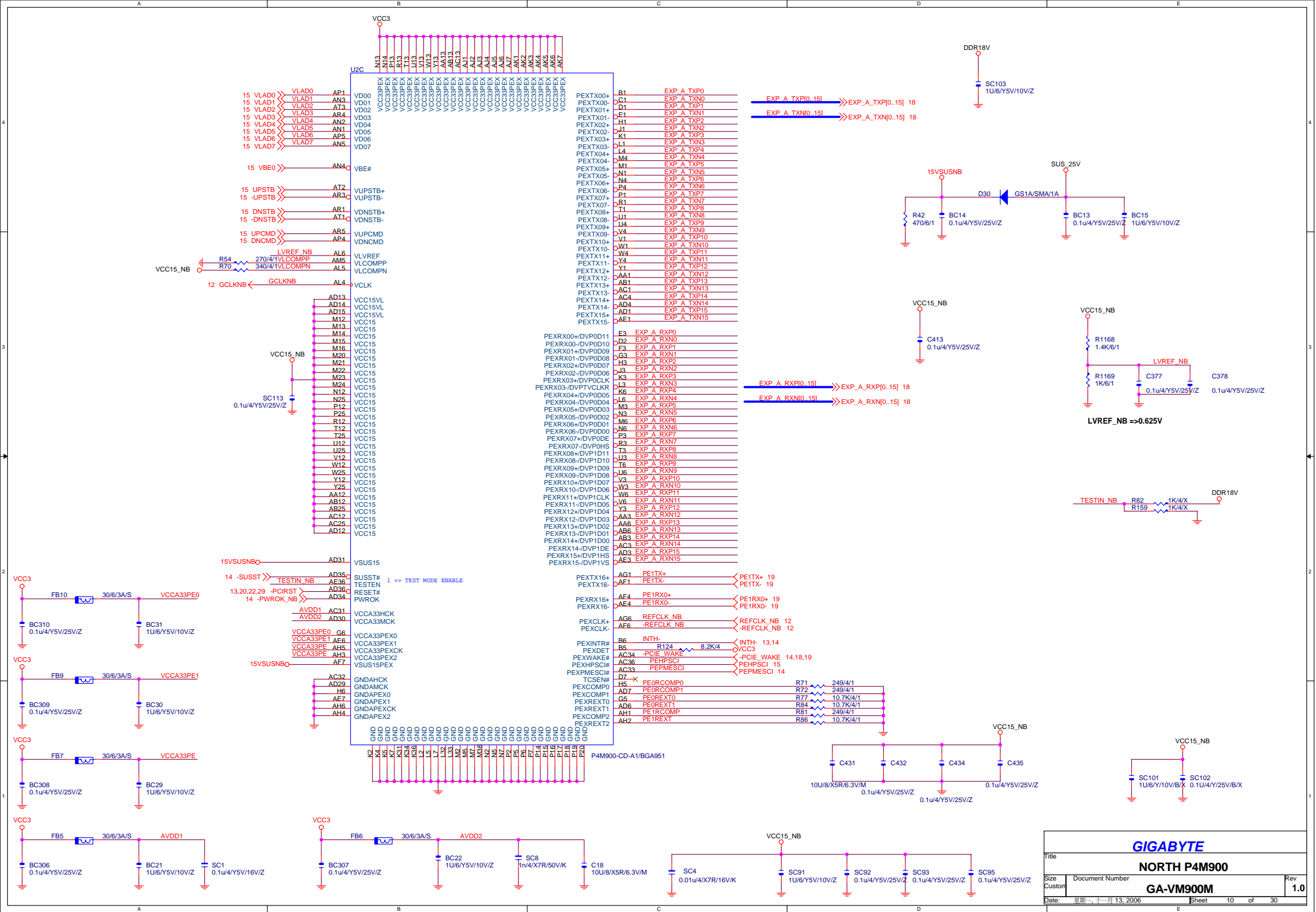
Asserted at 130 degree (RS2=720 ohm)  
Deasserted at 115 degree (RS2=1270 ohm)

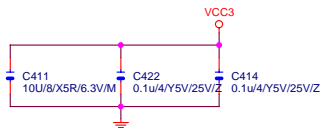
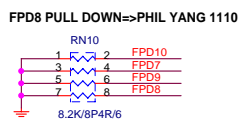
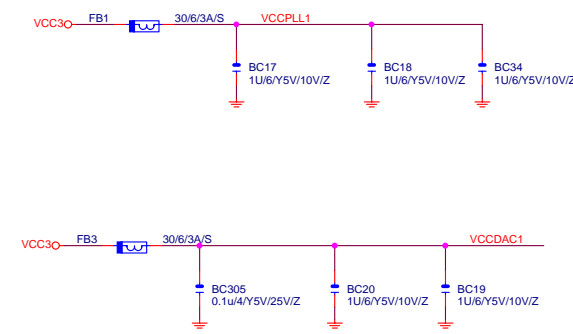
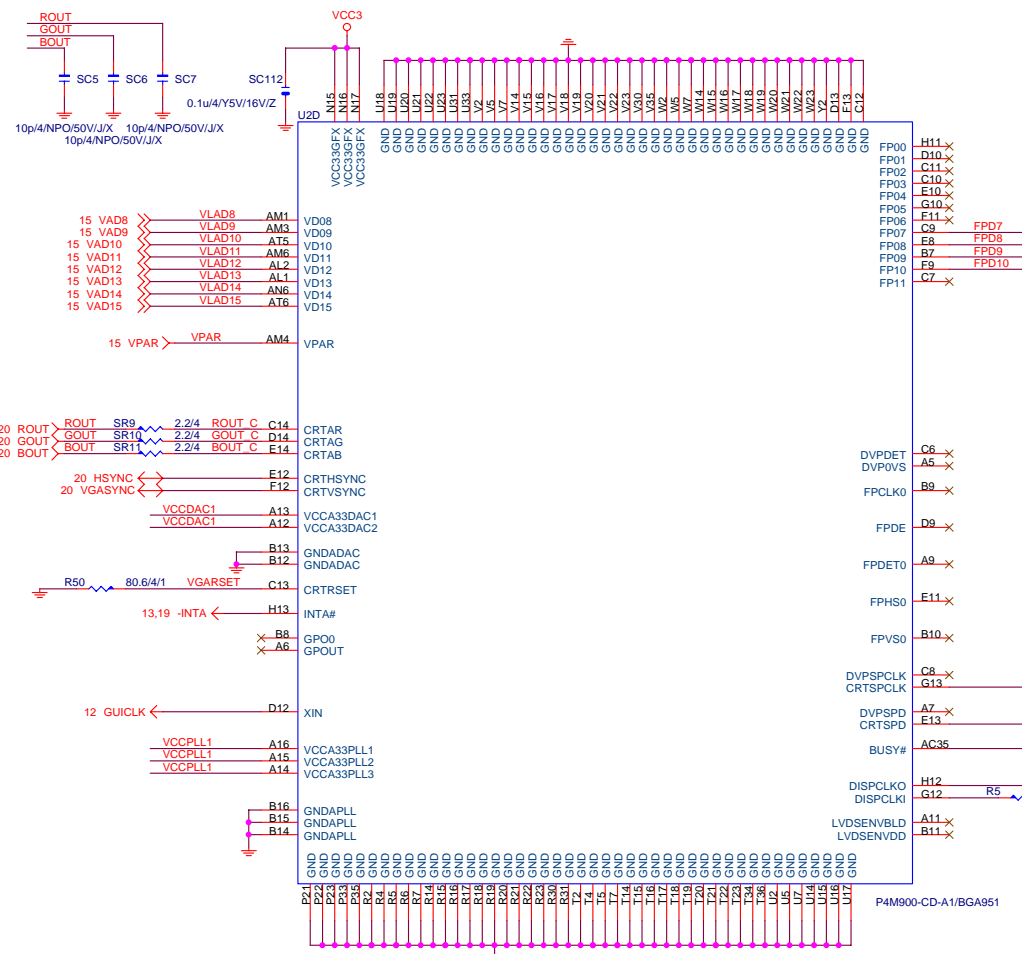




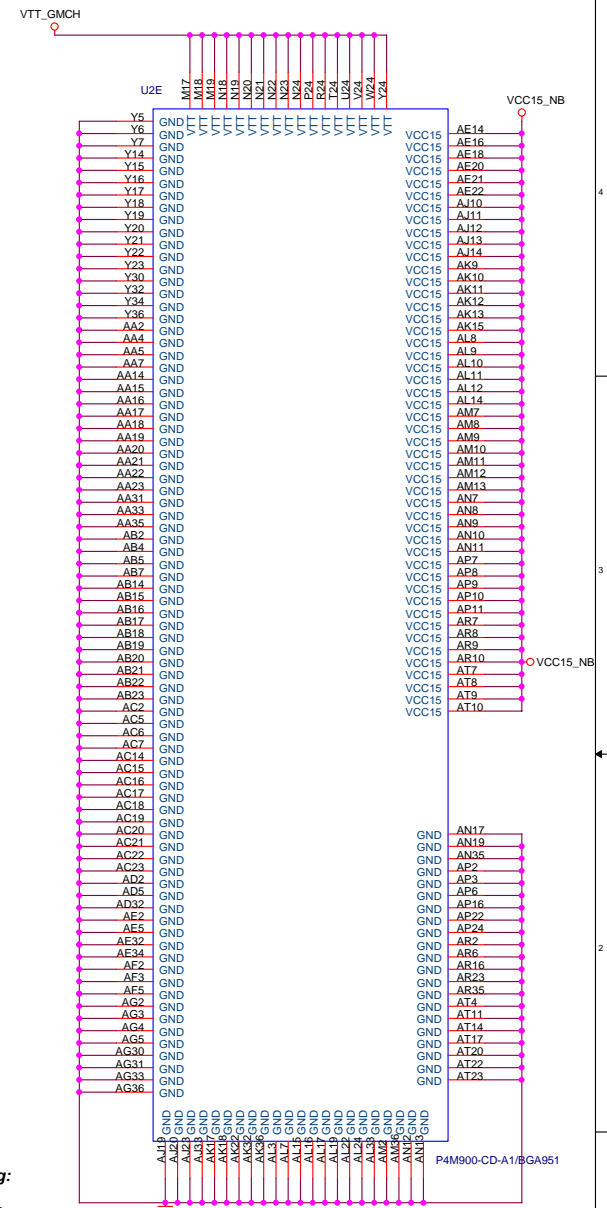








Check power

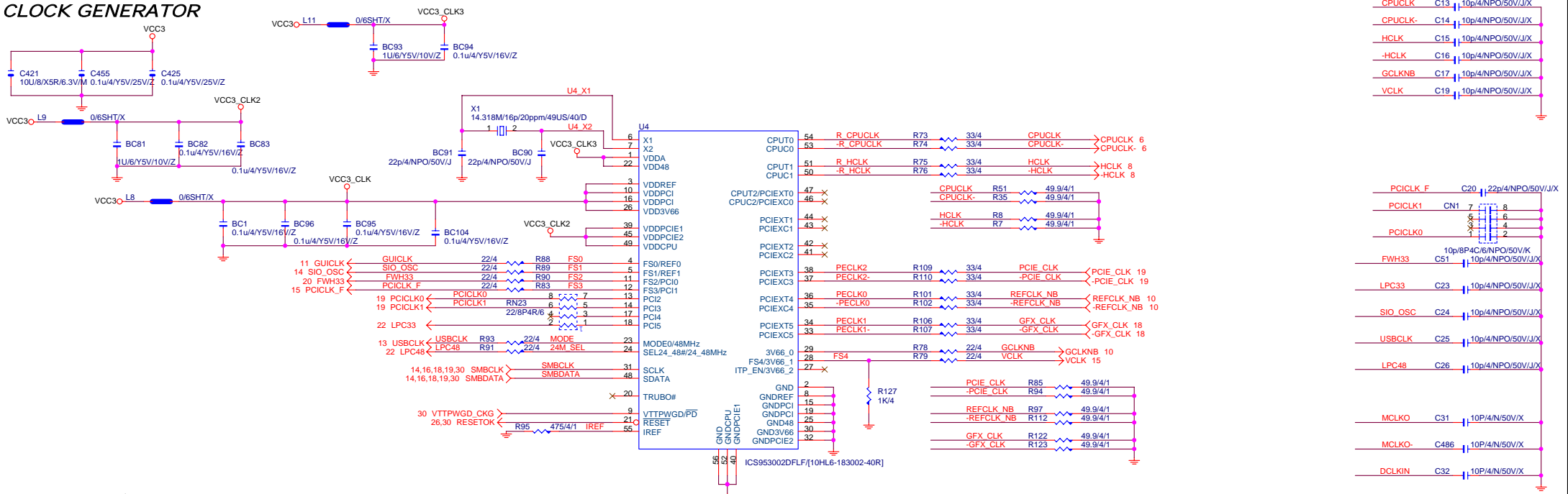


GFX power up strapping setting:

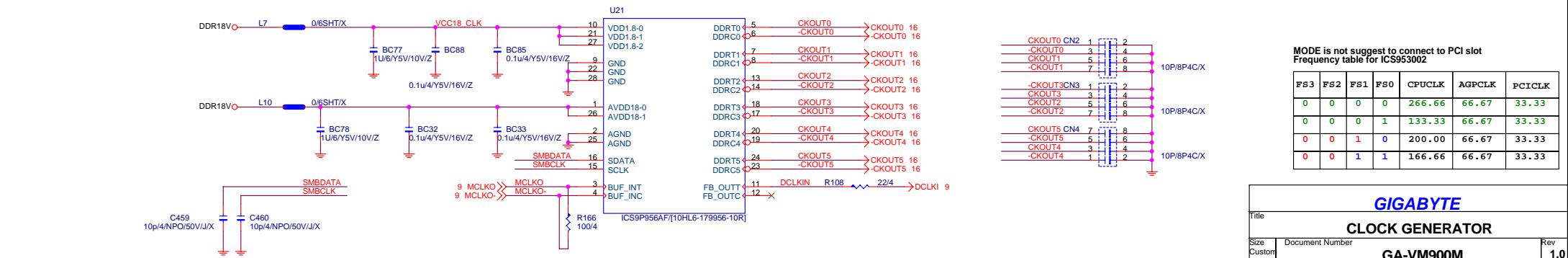
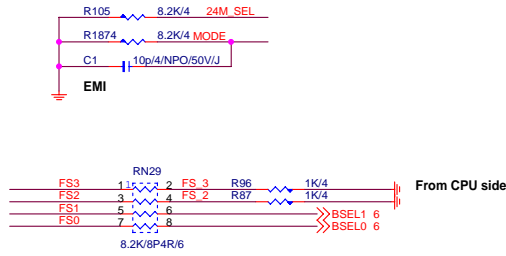
- TVD4/DVP0D4 =>AGP Port Muxing
  - 0: Two 12-bit DVI interface
  - 1: One 24-bit Panel Interface
- TVD5/DVP0D5 =>Dedicated DVI Port Configuration
  - 0: TMDS
  - 1: TV Encoder
- TVD6/DVP0D6 =>Dedicated DVI Port Selection
  - 0: Disable
  - 1: Enable
- TVD8/DVP0D8 =>External AGP Function Enable
  - 0: External
  - 1: Internal
- TVD9/DVP0D9 =>PCI Signal Test Output Enable
  - 0: Disable
  - 1: Enable
- TVD10/DVP0D10 =>CPUCK/MCK Clock Select
  - 0: From NB
  - 1: From External
- TVD7/DVP0D7 =>GTX Clock Select(VCK/LCDCK/ECK)
  - 0: Refer Internal PLL
  - 1: From External

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NORTH P4M900			
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## CLOCK GENERATOR

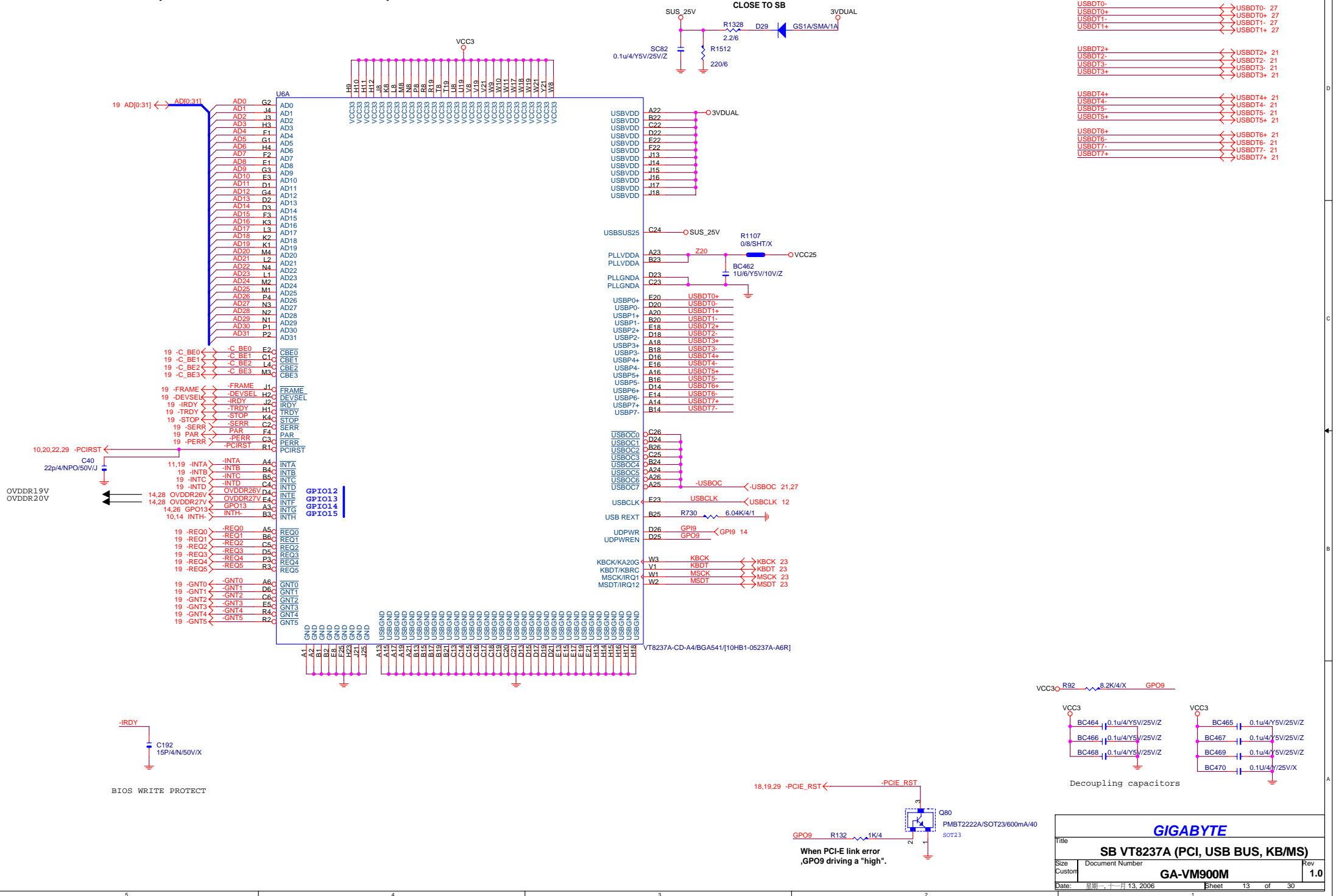


1. 3VDUAL 是否漏電
2. VTTPWOK control 25M or other ?
3. Any 56pin CKG w/s 25M & 24.576M ?
4. DDR18V 是否漏電 , Latch 靠誰?
5. DDR18V output enable 靠power or VTTPWOK ?
6. S3 & S5 那些clock 會output ?



FS3	FS2	FS1	FS0	CPUCLK	AGPCLK	PCICLK
0	0	0	0	266.66	66.67	33.33
0	0	0	1	133.33	66.67	33.33
0	0	1	0	200.00	66.67	33.33
0	0	1	1	166.66	66.67	33.33

***SB VT8237R+ (PCI, USB BUS, KB/MS)***



# SB VT8237R+ (SATA,IDE, AC97, POWER MANAGEMENT, PGIO)

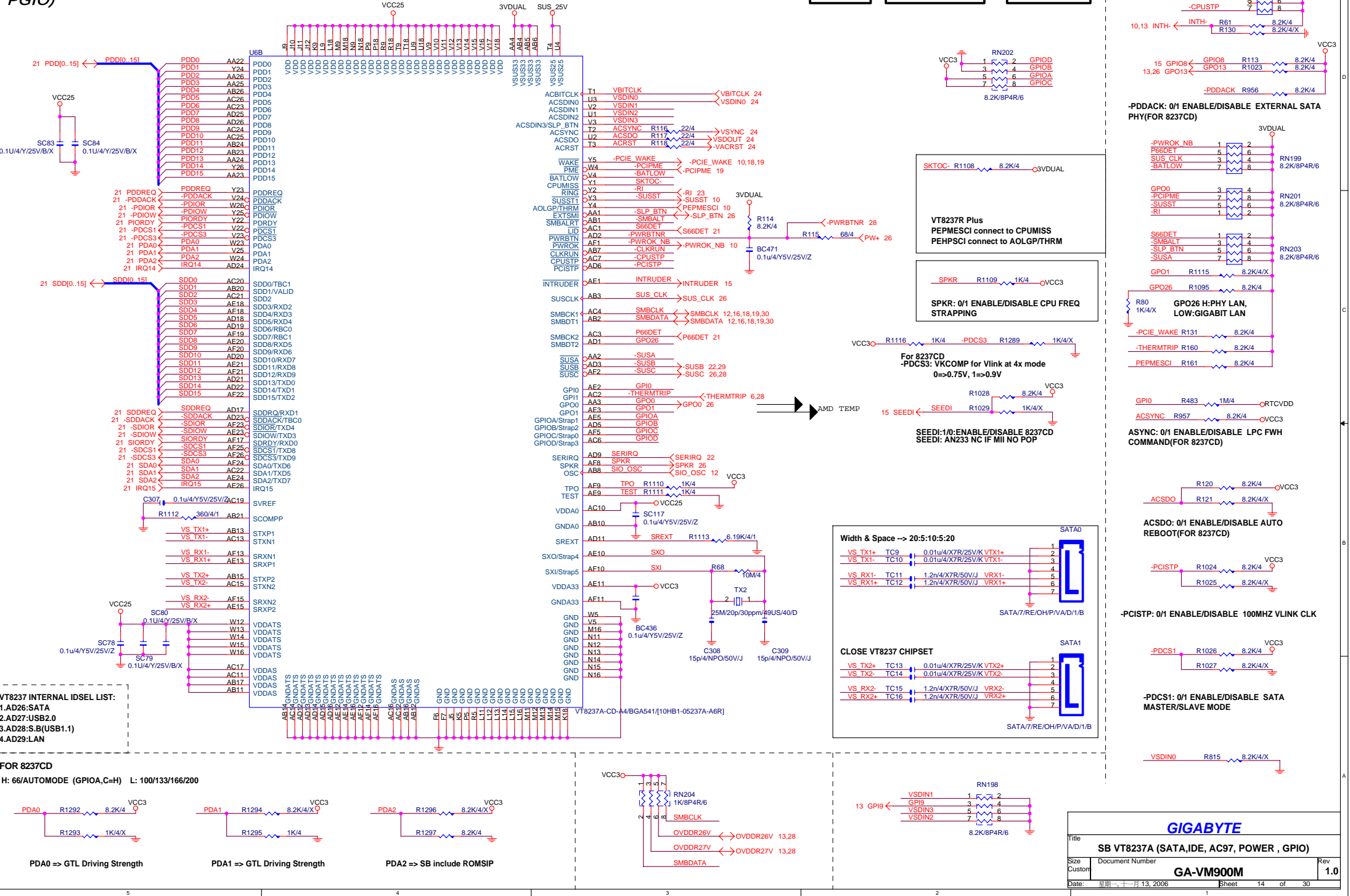
GPIOA Vlink auto compenstaion  
0 -> Auto Mode 1=Manual Mode

GPIOB  
0 -> IOQ=8  
1 -> IOQ=1

GPIOC -HOST CLOCK  
0 -> 200MHz 1 ->  
Auto MODE

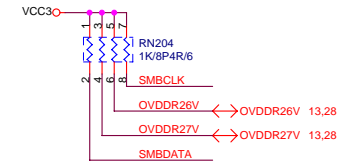
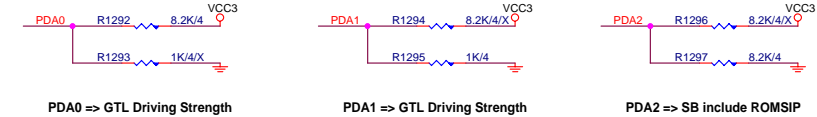
GPIOD = GTL Pull  
0 -> Enable  
1 -> Disable

GPIO ID SETTING  
SERIRQ -> SERIRQ  
-CLKRUN -> CLKRUN  
-CPUSTP -> CPUSTP



VT8237 INTERNAL IDSEL LIST:  
1.AD26:SATA  
2.AD27:USB2.0  
3.AD28:S.B(USB1.1)  
4.AD29:LAN

FOR 8237CD  
H: 66/AUTOMODE (GPIOA,C=H) L: 100/133/166/200



GIGABYTE			
SB VT8237A (SATA,IDE, AC97, POWER , GPIO)			
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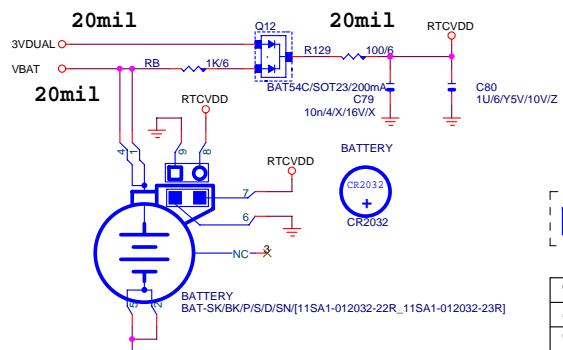
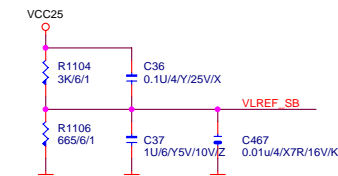
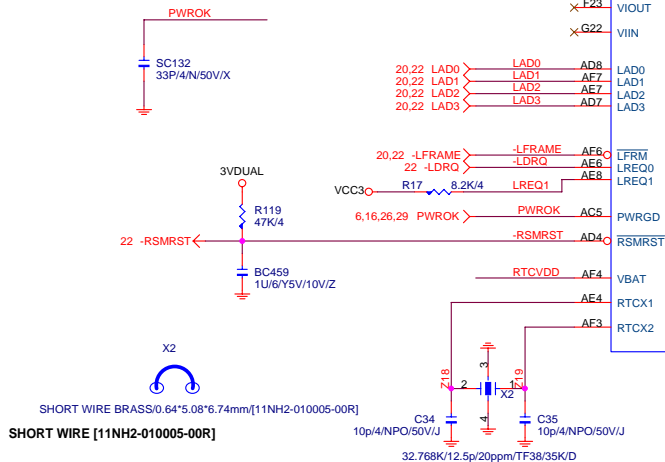


# SB VT8237R Plus (Vlink, CPU, LPC, LAN, LAN EEPROM, I2C BUS)

VLAD, STRBOE, CMD mismatch <100 mil

LVREF\_NB, LVREF\_SB, LCOMP, VCOMP as wide as possible.

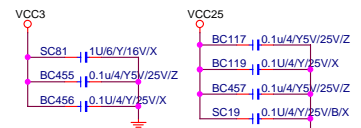
STRBOE mismatch <25 mil



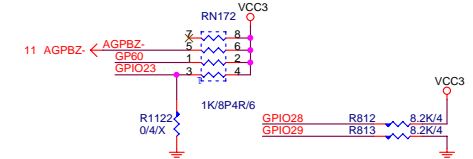
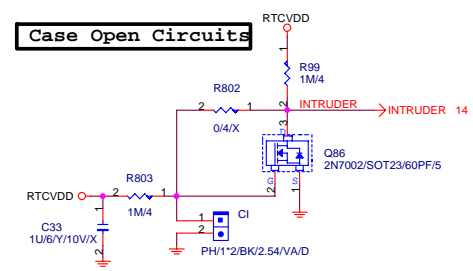
CLR\_CMOS  
PH1\*2BK/2.54VA/D:[8-9]POP

CLR_CMOS	CLEAR COMS JUMPER
SHORT	CLEAR CMOS
OPEN	NORMAL (Default)

## Decoupling capacitors

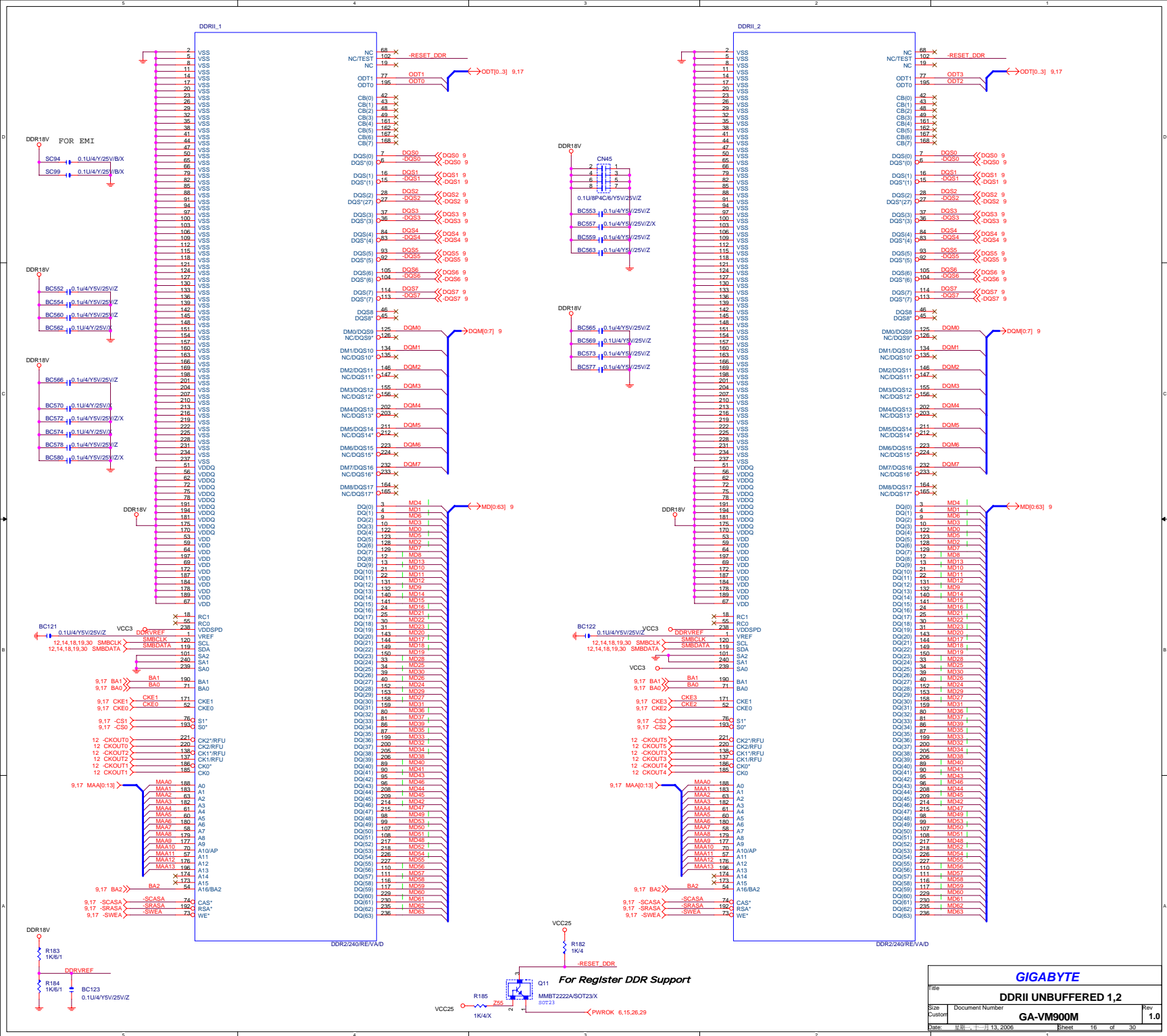


## Case Open Circuits

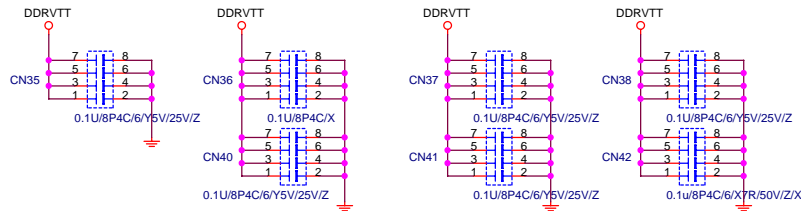


## GIGABYTE

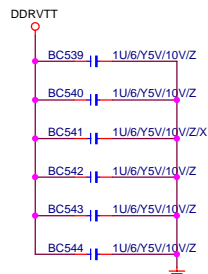
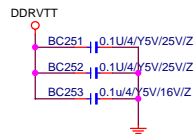
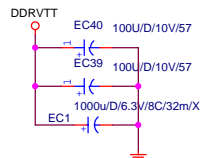
Title	SB VT8237A (Vlink, CPU, LPC, LAN, I2C)		
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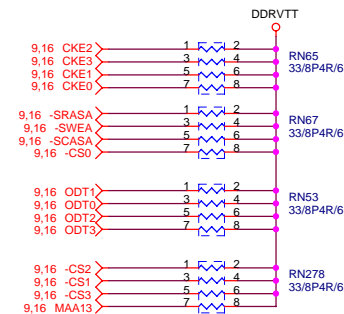
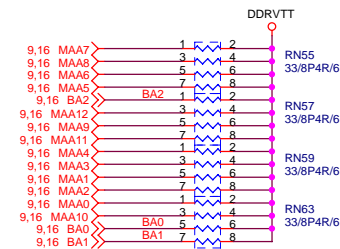
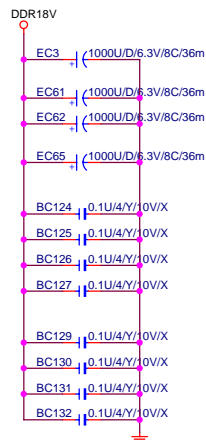


## DDRVTT Decouple



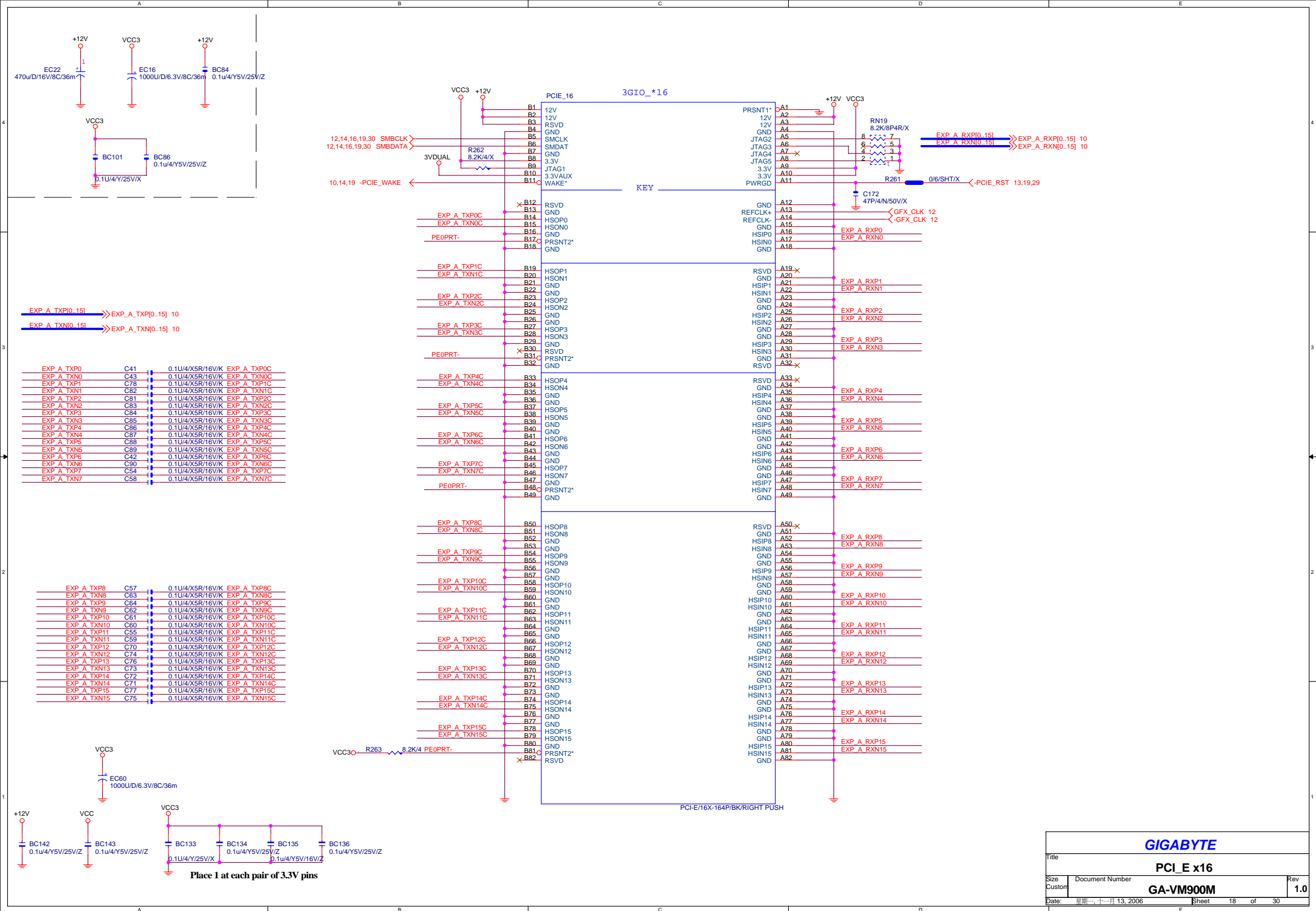
NOTE: Place these decoupling capacitors close to VTT\_MEM termination resistors. (one decoupling capacitor for each two R-packs)

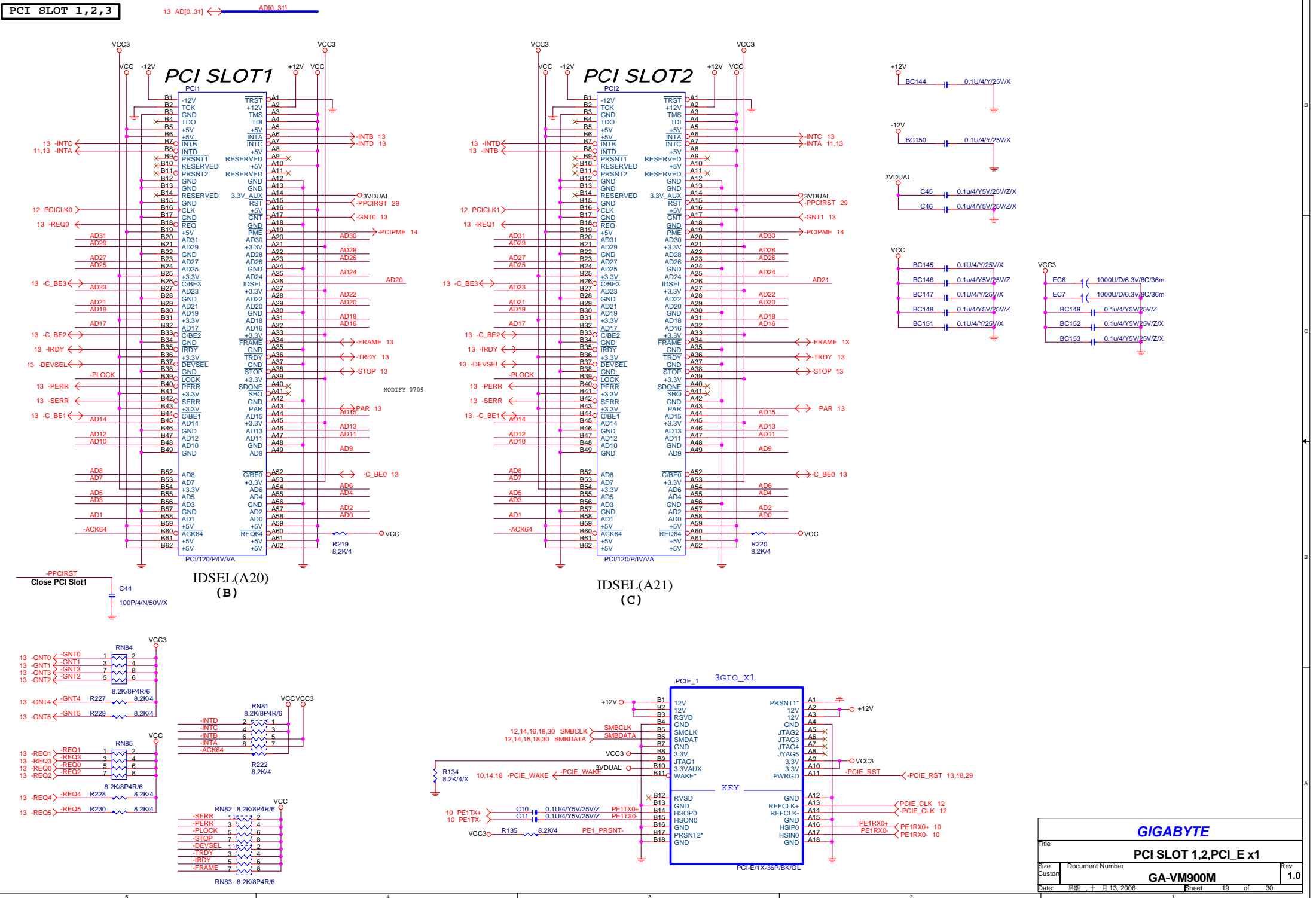
## DDR18V Decouple



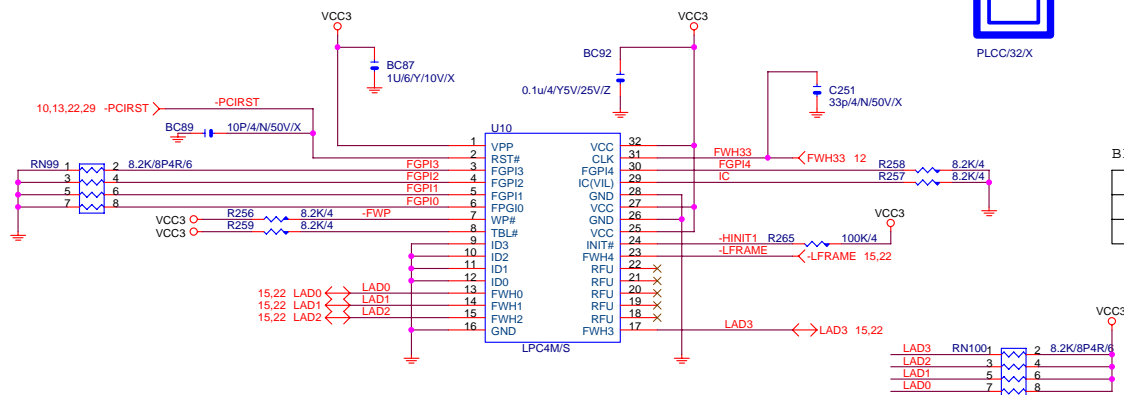
**GIGABYTE**

Title			DDRII Terminator		
Size			Document Number		
Custom			GA-VM900M		
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Title			
GIGABYTE			
PCI SLOT 1,2,PCI_E x1			
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Custor			
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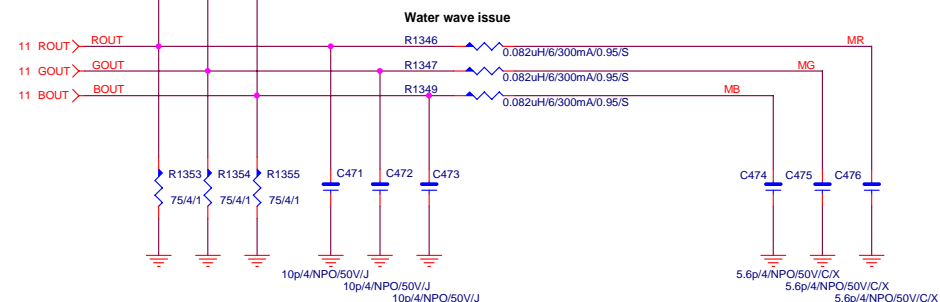
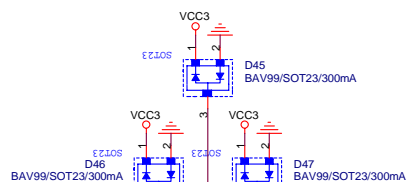
BIOS\_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE

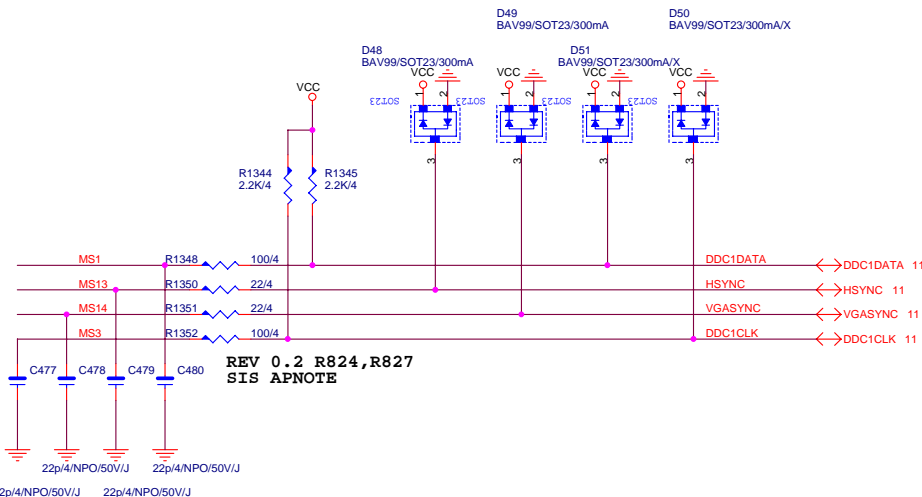
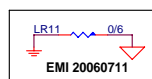
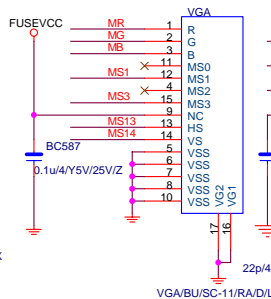
BIOS\_WP\_SHUNTER



SHUNTER/2-3/G/X



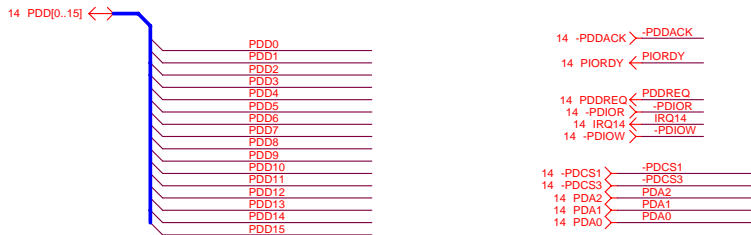
% PLEASE PLACE THESE COMPONENTS AS NEAR VGA CONNECT AS POSSIBLE



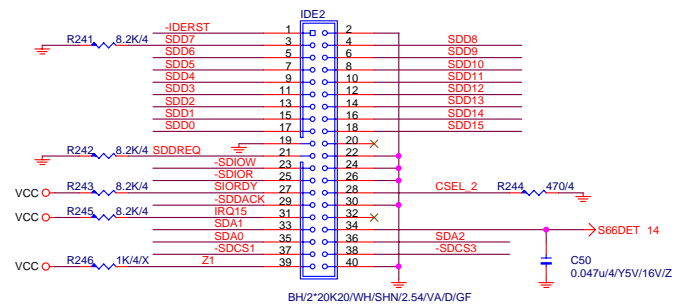
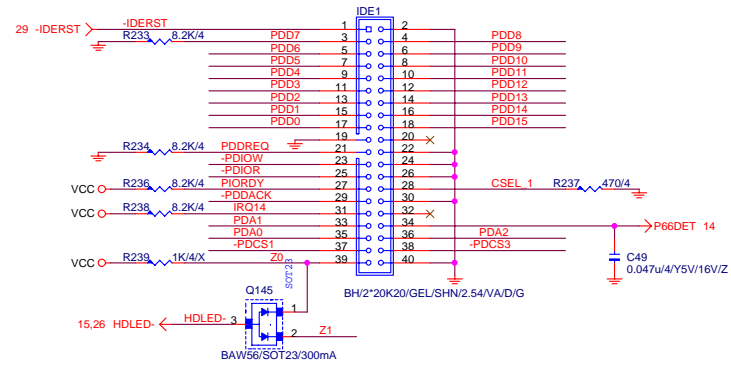
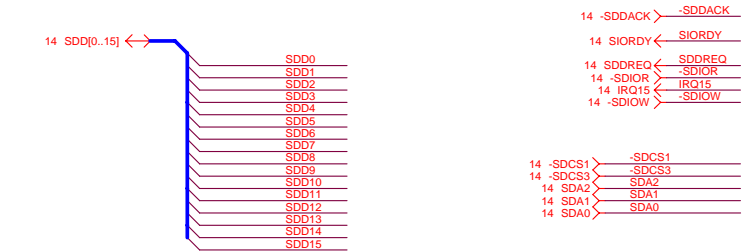
REV 0.2 R824,R827  
SIS APNOTE

GIGABYTE			
Title			
BIOS & VGA CONN			
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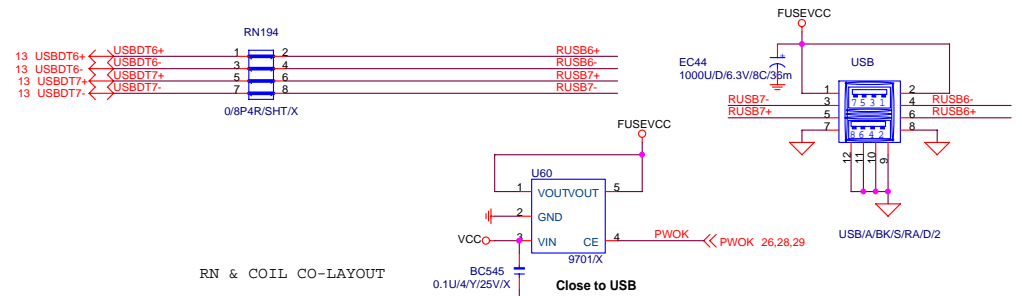
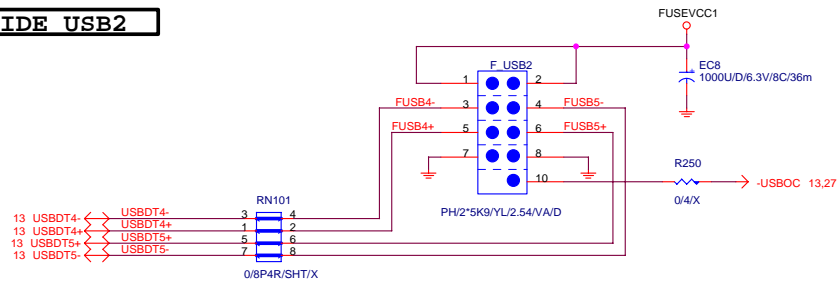
## PRIMARY IDE



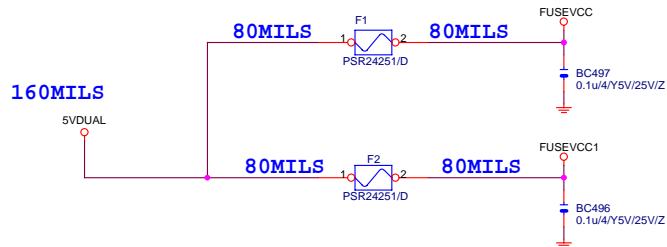
## SECONDARY IDE



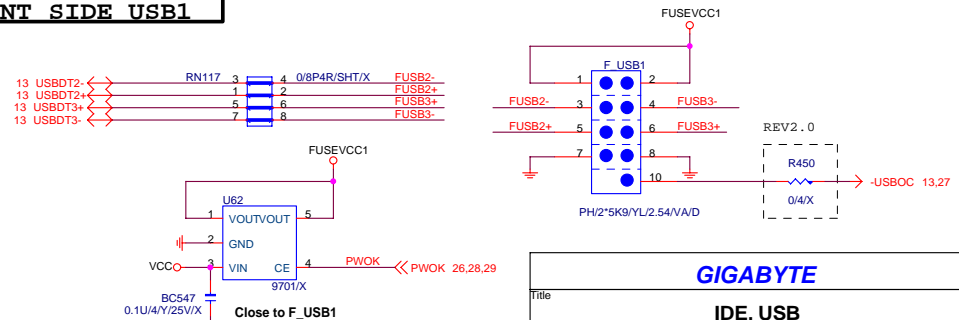
## FRONT SIDE USB2



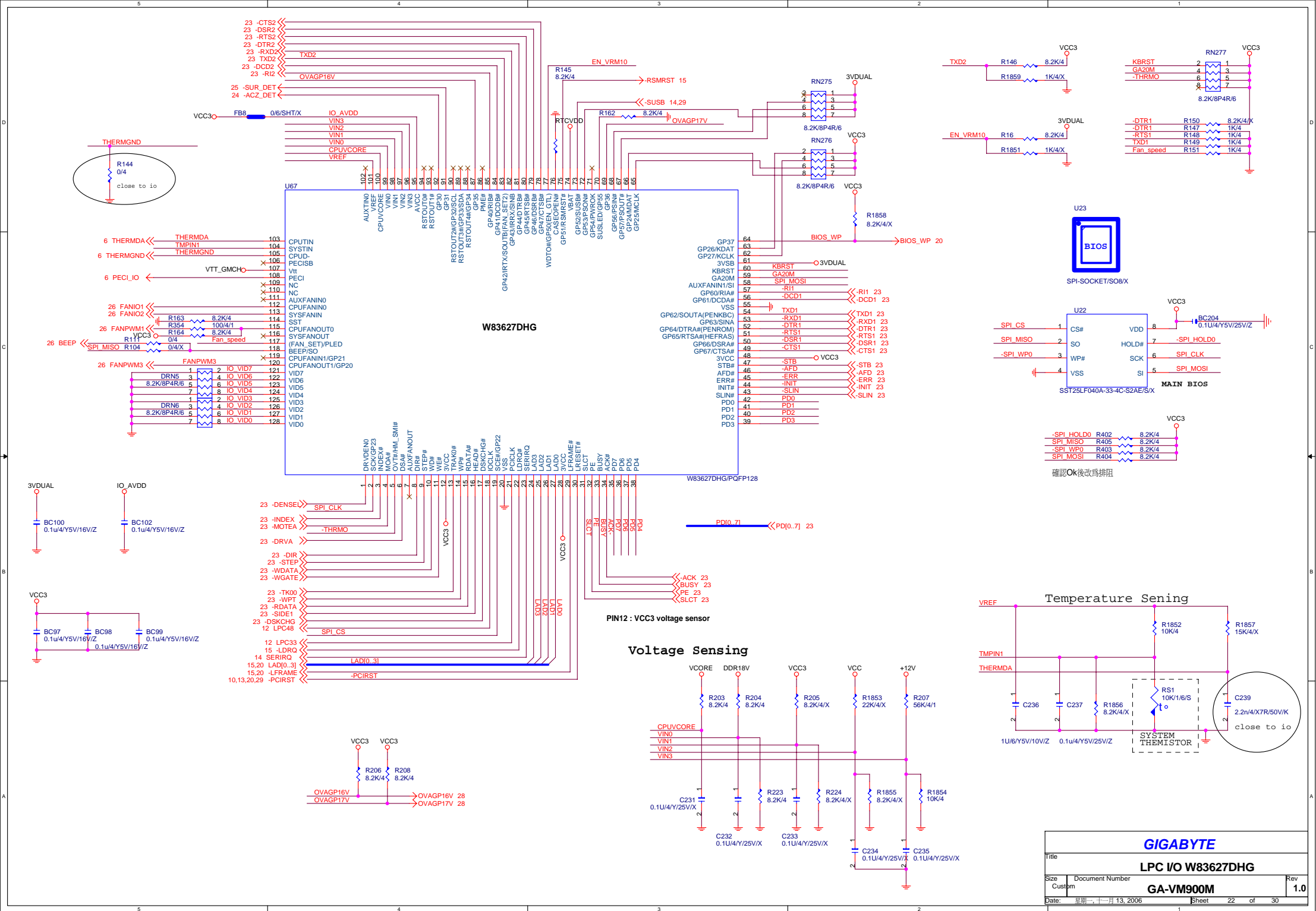
## FUSEVCC



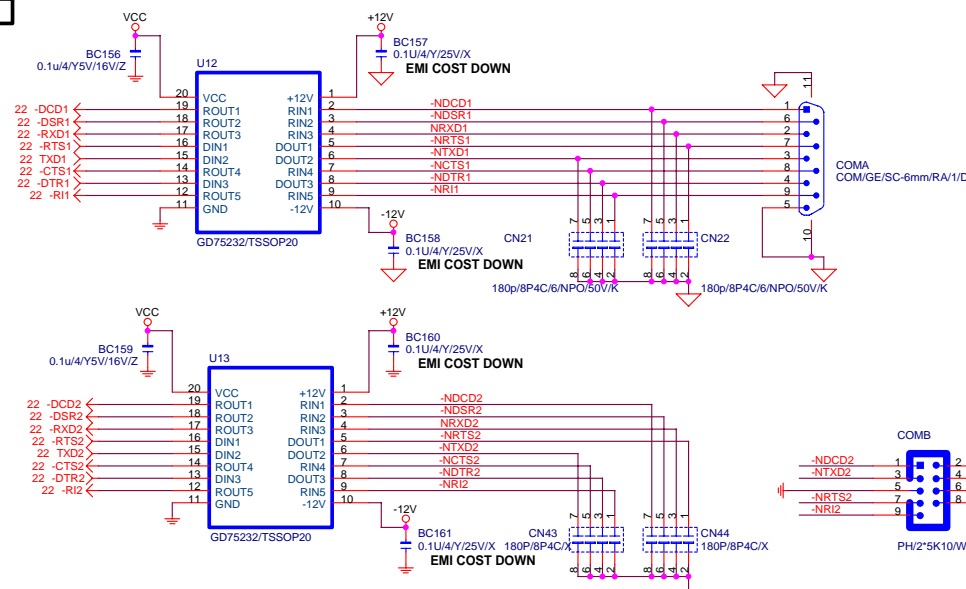
## FRONT SIDE USB1



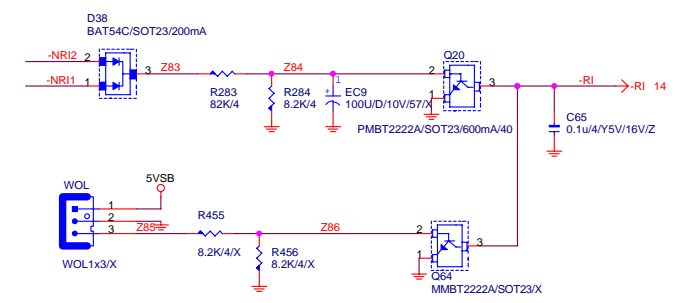
GIGABYTE		
Title		
IDE, USB		
Size	Document Number	Rev
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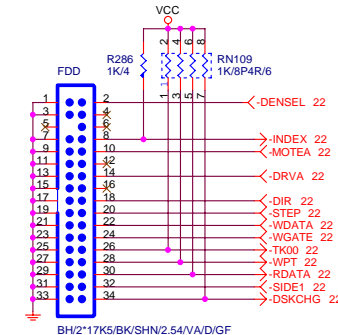
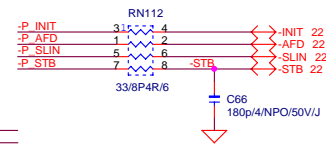
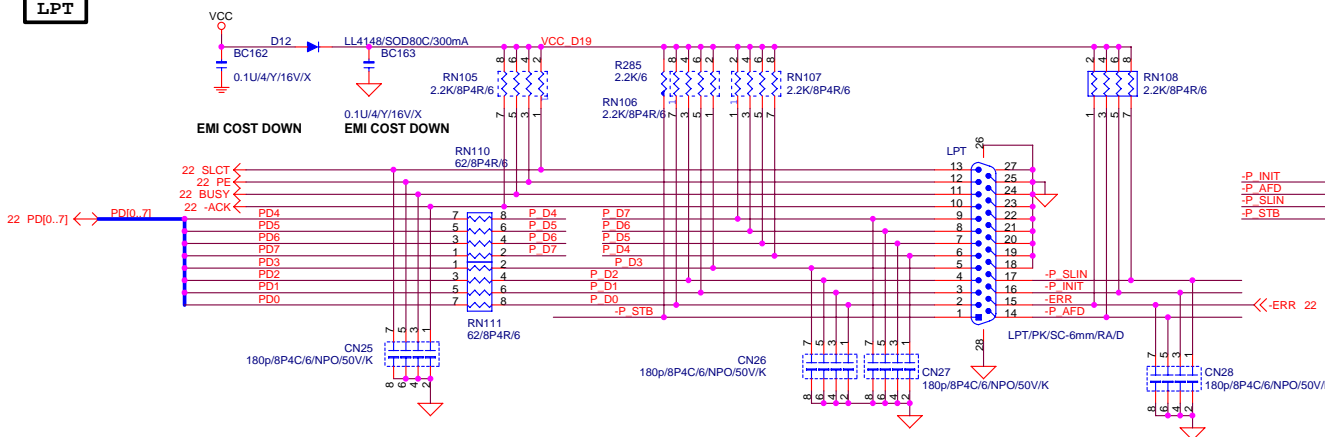
# COM A, B



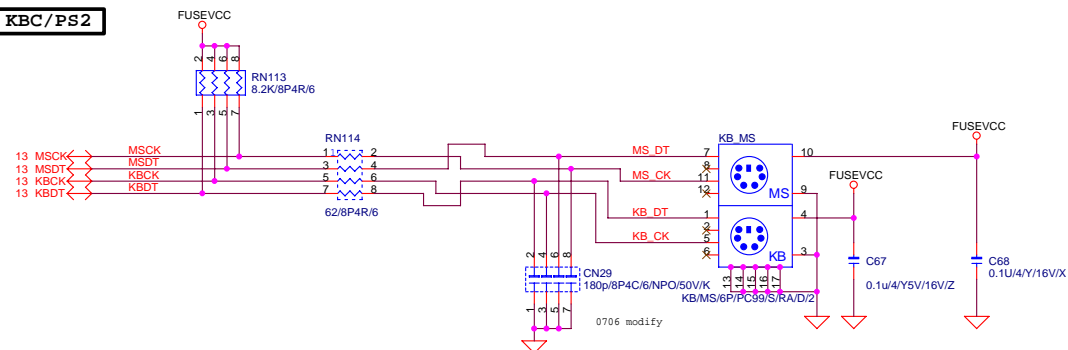
# WAKE UP



# LPT



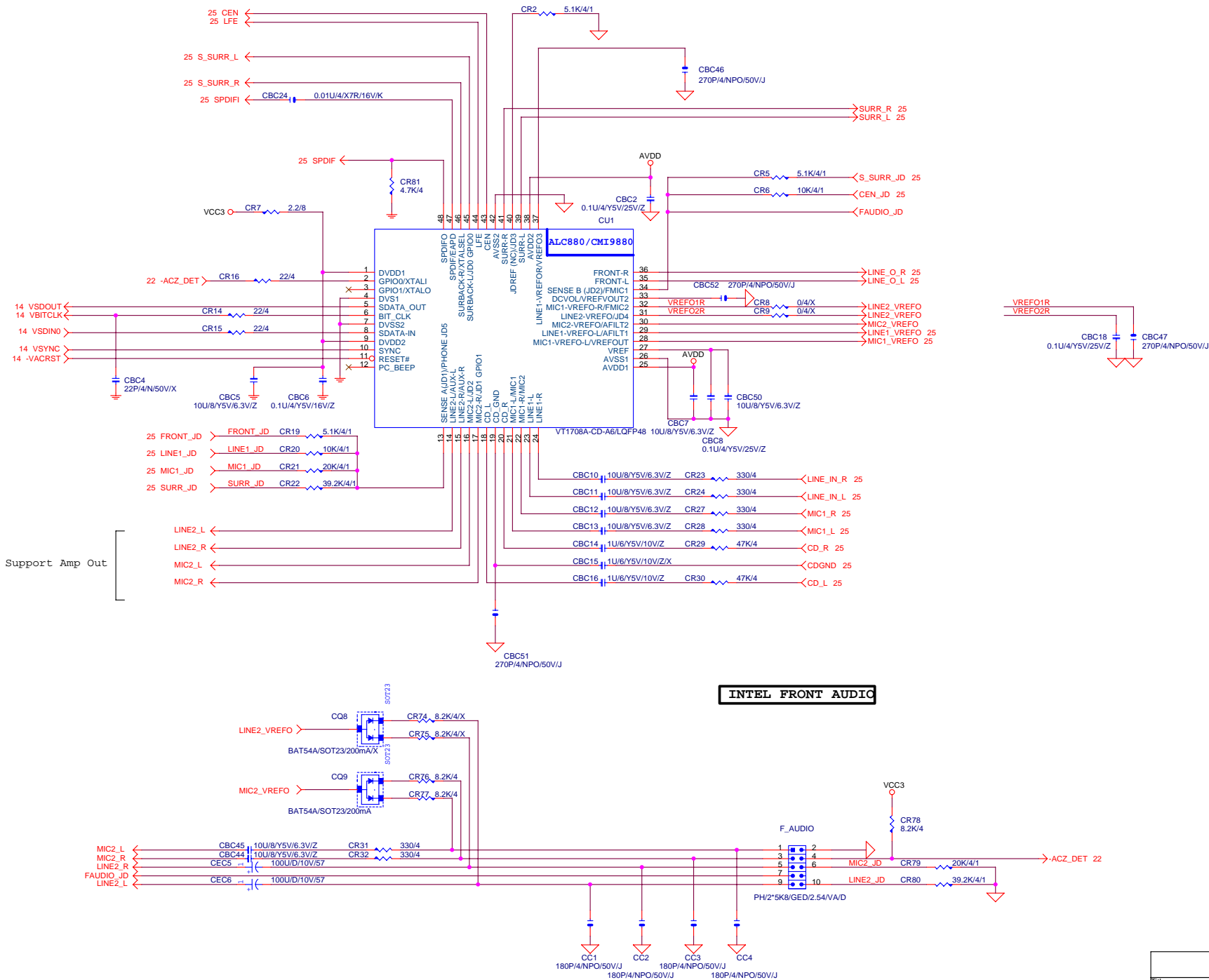
# KBC/PS2



GIGABYTE			
COM,PRT,FDD,KB			
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Can Support Amp Out

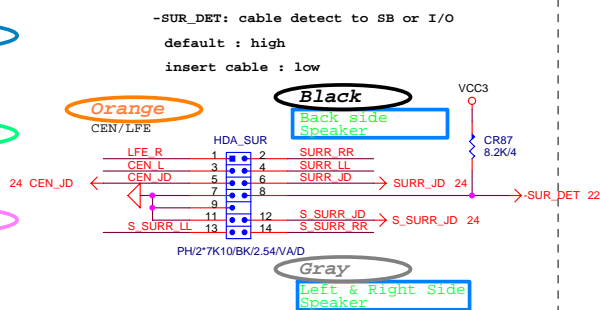
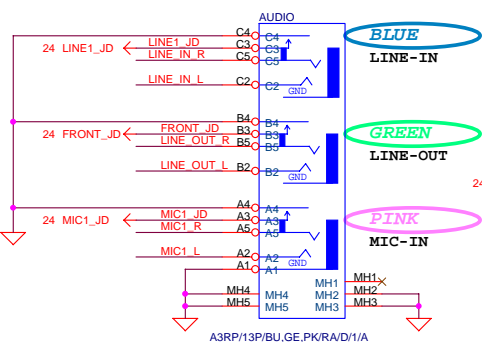
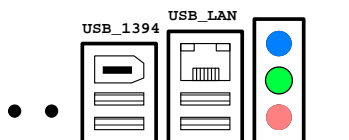
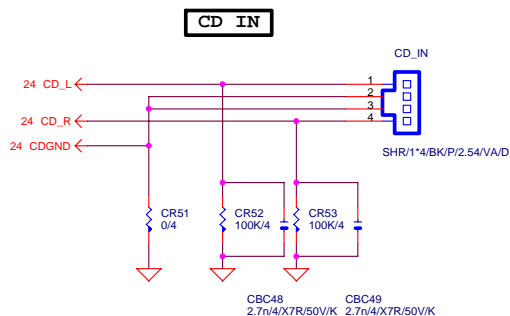
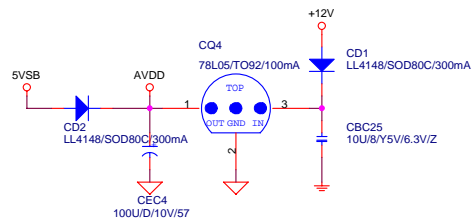
### INTEL FRONT AUDIO



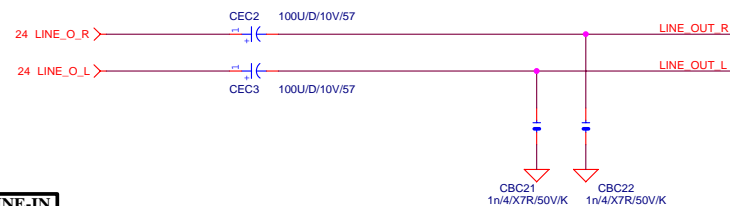
GIGABYTE

Title			VT1708A CODEC
Size			Document Number
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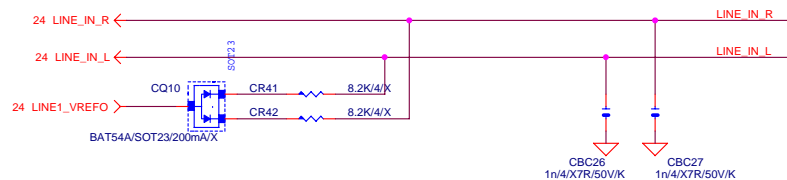




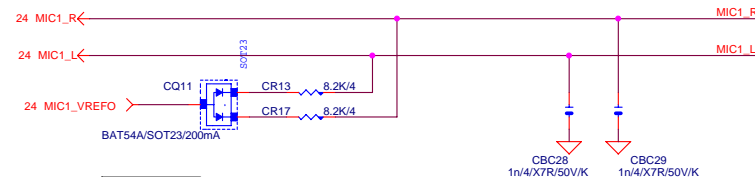
LINE OUT  
FRONT OUT



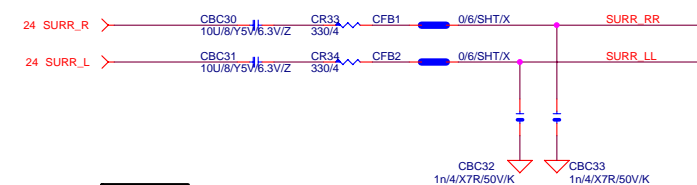
### LINE-IN



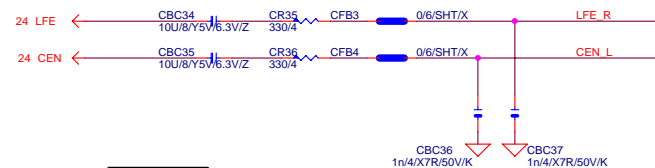
MIC



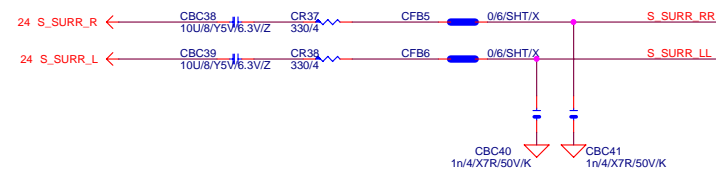
**SURROUND**



## CEN/LFE

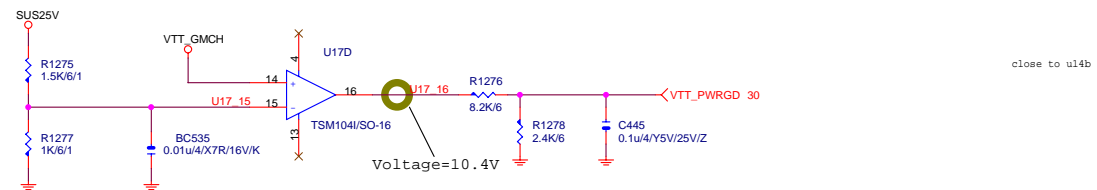
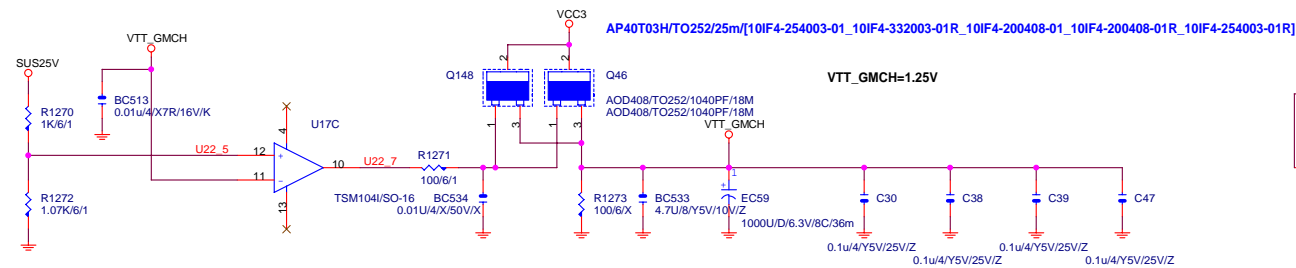


**SURR BACK**

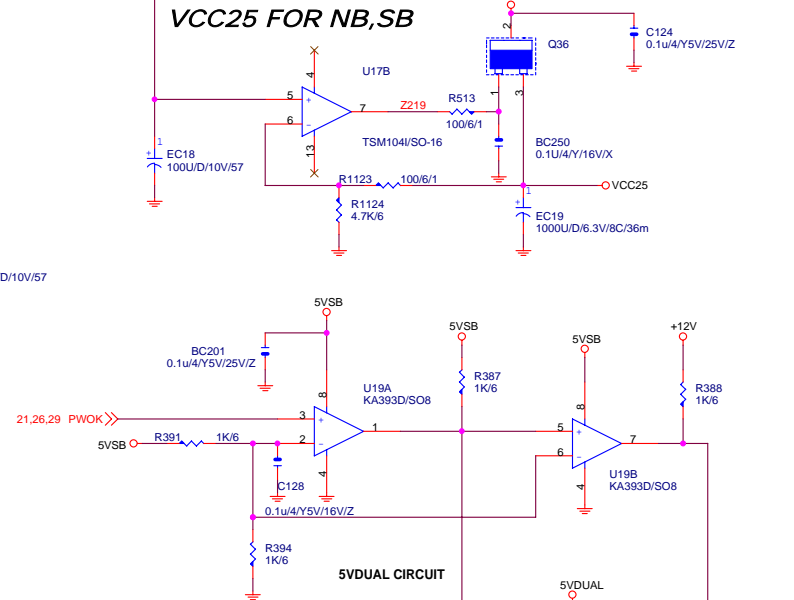
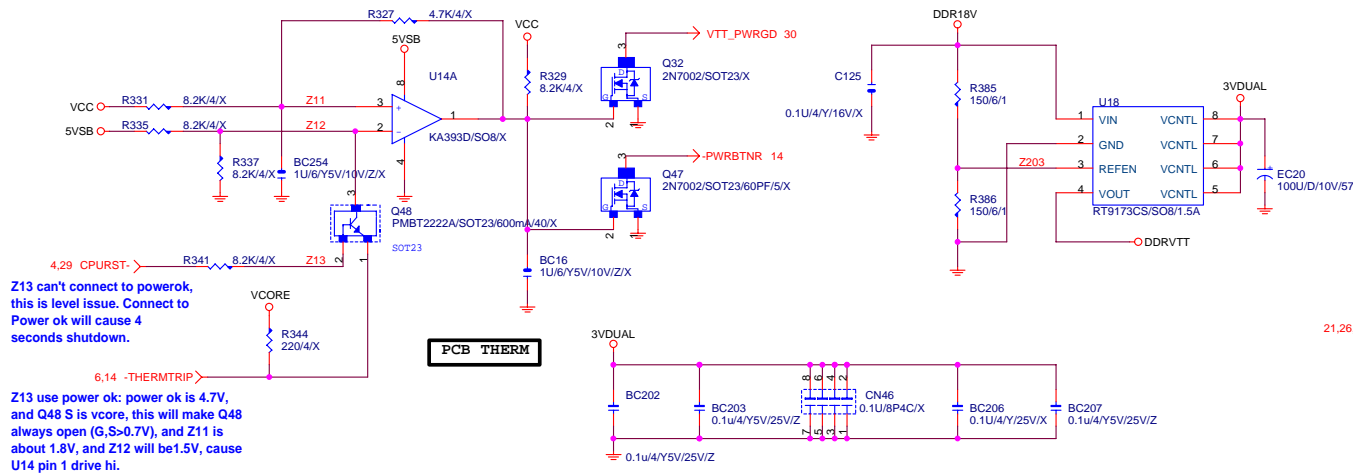




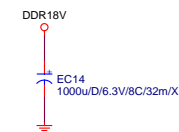
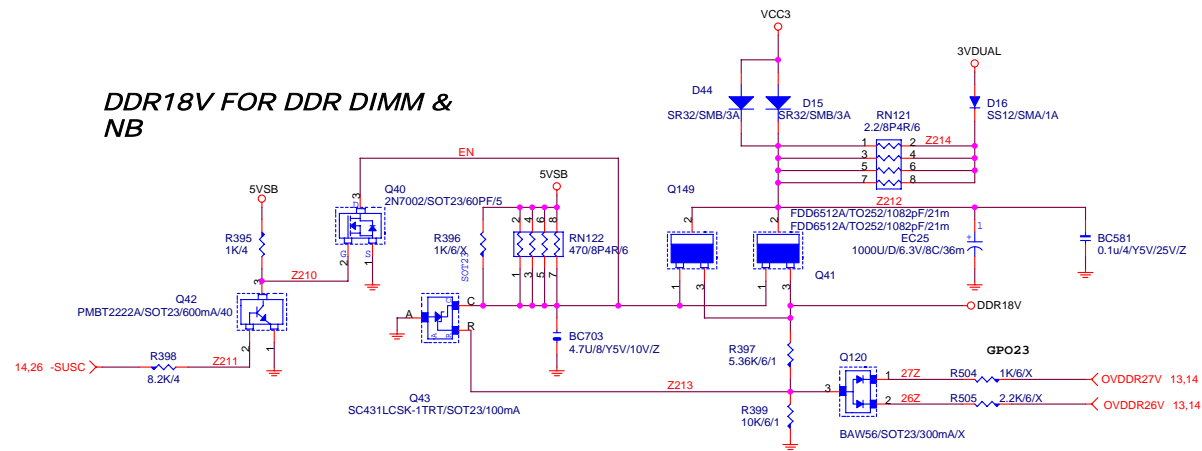




### 0.9V DDRVTT SWITCHING SOLUTION



**DDR18V FOR DDR DIMM & NB**



## ATX CONN, DC POWER

## ATX POWER CONNECTOR

